CERTIFICATES OF COMPETENCY IN THE MERCHANT NAVY
MARINE ENGINEER OFFICER

STCW 78 as amended MANAGEMENT ENGINEER REG. III/2 (UNLIMITED)

040-33 - ELECTROTECHNOLOGY

THURSDAY, 21 OCTOBER 2021

0915 - 1215 hrs

Materials to be supplied by examination centres

Candidate's examination workbook Graph paper

Examination Paper Inserts

Worksheet Q5

1. Examinations administered by the SQA on behalf of the Maritime & Coastguard Agency.
2. Candidates should note that 96 marks are allocated to this paper. To pass, candidates must achieve 48 marks.
3. Non-programmable calculators may be used.
4. All formulae used must be stated and the method of working and all intermediate steps must be made clear in the answer.

Maritime & Coastguard Agency

SQA

ELECTROTECHNOLOGY

Attempt SIX questions only.

All questions carry equal marks.

Marks for each part question are shown in brackets.

1. Fig Q1 shows a d.c. ring main supplied by two 230 V generators. The cable section resistances are for go and return.

Calculate EACH of the following:

(a) the current in each cable section; (7)

(b) the power loss in each cable section; (6)

(c) the voltage at each load. (3)

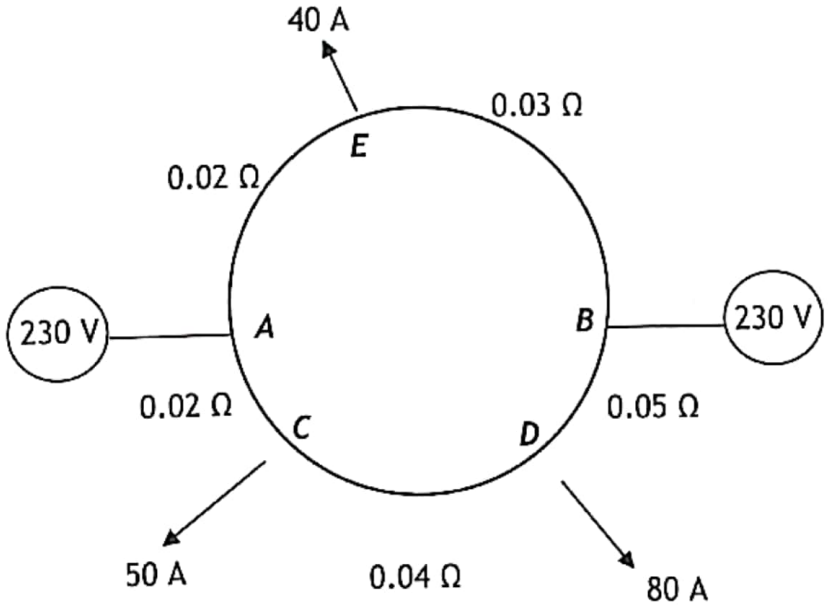

Fig Q1

2. A capacitor of 100 μF is charged from a 120 V d.c. supply via a 100 kΩ resistor for 4 seconds.

(a) Calculate EACH of the following:

(i) the time constant of the circuit; (2)

(ii) the voltage to which the capacitor has charged after 4 seconds. (4)

(b) A second capacitor of 80 μF is now charged for 4 seconds from the same supply via the same 100 kΩ resistor. Both charged capacitors are now disconnected from the supply and then connected in parallel.

Calculate EACH of the following:

(i) the final steady state voltage across the pair of capacitors; (8)

(ii) the total energy stored in the two capacitors. (2)

3. Three identical coils are connected in delta across a three-phase power supply. The load takes a line current 15 A from the supply, consumes 7.5 kW and develops 10 kVA.

Calculate EACH of the following for the load:

(a) the line and phase voltages; (3)

(b) the impedance per phase; (3)

(c) the power factor; (2)

(d) the reactance per phase; (5)

(e) the resistance per phase; (1)

(f) the inductance per phase if the frequency is 60 Hz. (2)

4. A three-phase electrical load of 1000 kW is operating at a power factor of 0.6 lagging. The supply power factor is improved to 0.95 lagging by connecting a synchronous motor driving a load of 300 kW with an efficiency of 93%.

Calculate EACH of the following:

(a) the kVA of the synchronous motor; (14)

(b) the power factor of the synchronous motor. (2)

5. Fig Q5 shows a single-line diagram of a ship's electrical power system:

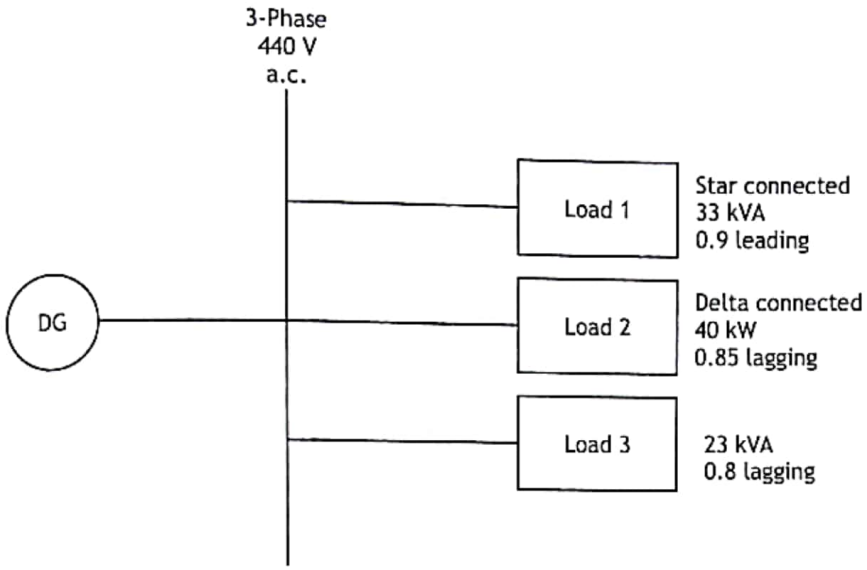

Fig Q5

(a) Determine and insert the missing data in the Worksheet Q5. (8)

(b) Calculate EACH of the following:

(i) the kVA supplied by DG; (2)

(ii) the current supplied by DG; (2)

(iii) the phase current for Load 1 and the phase current for Load 2. (4)

6. (a) With reference to power transformers, explain EACH of the following statements:

(i) core losses are fixed; (2)

(ii) copper losses are variable. (2)

(b) A 60 kVA, 440 V/110 V single-phase transformer has iron loss of 4 kW, and a full load copper loss of 6 kW.

Calculate EACH of the following:

(i) the kVA output at which maximum efficiency will be achieved; (4)

(ii) the efficiency at 50 kW output and 0.85 p.f. (8)

[OVER

7. (a) Explain the meaning of the term *power factor*. (3)

(b) State TWO advantages of power factor correction. (4)

(c) Explain, with the aid of a circuit diagram, how power factor correction can be achieved in a three phase circuit using capacitors. (5)

(d) Explain ONE method, other than the use of capacitors, by means of which power factor correction can be achieved. (4)

8. With reference to a variable frequency drive (VFD) system:

(a) explain why it is essential to maintain the *v/f* ratio of the power supply; (3)

(b) sketch a labelled block diagram of a typical electronic VFD scheme; (4)

(c) describe, with the aid of a circuit diagram, the operation of a three-phase rectifier; (5)

(d) describe a controlled inversion process. (4)

9. (a) Describe, with the aid of a sketch, the operation of a *p-n* junction diode in EACH of the following states:

(i) the forward bias; (4)

(ii) the reverse bias. (4)

(b) A centre-tapped full-wave rectifier employing an ideal diode has an r.m.s. half-secondary voltage of 9 V.

If the load resistance is 1 kΩ, calculate EACH of the following:

(i) the peak current; (4)

(ii) the d.c. load voltage. (4)